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(54) TEMPERATURE COMPENSATION TYPE ELECTRONIC TIMEPIECE

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SPECIFICATION

1. TITLE OF THE INVENTION

TEMPERATURE COMPENSATION TYPE ELECTRONIC TIMEPIECE

2. CLAIMS

Temperature compensation type electronic timepiece comprising: a highly accurate electronic timepiece having a temperature detected circuit, an A-D converter in which analog temperature information is converted into digital information, and a temperature information correction circuit for correcting the variance of the digital information; and

wherein the temperature compensation type electronic timepiece further having a storage circuit which supplies a corrected value to the temperature information correction circuit, a logical circuit which generates a first and a secondary coefficient for the output data of the temperature

information correction circuit and temperature, a oscillation circuit varies frequency according to the output data of the logical circuit, and a frequency dividing circuit for performing logical speeding-up and slowing-down operation according to the another output data of the logical circuit.

3. DETAILED DESCRIPTION OF THE INVENTION

[TECHNICAL FIELD]

The present invention relates to a highly accurate electronic timepiece by correcting frequency deviations due to a temperature of a quartz-crystal oscillator.

[DESCRIPTION OF RELATED ART]

FIG. 1 shows a block diagram for a conventional temperature compensation type highly accurate timepiece circuit. An analog information in proportion to the temperature in a temperature detecting circuit 103 is converted into a digital information by an A-D converting circuit 104. Thereafter, the temperature detecting circuit has the variance respectively, which is corrected by a temperature information correction circuit. With 32 kHz quartz-crystal oscillator for the timepiece, since the secondary coefficient has greatly affect to the temperature, square circuit is formed by a pulse width modulation circuit 106 so as to vary the oscillation frequency of a crystal oscillation circuit.

However, since the temperature information is feedback to the oscillation circuit as they are to perform a large capacity switching, the circuit becomes not stable, therefore, the wide-range temperature compensation has been difficult. Also, in the crystal, since a tertiary characteristic to the temperature is included, when the temperature is equal to or more than the

normal temperatures with plus or minus 20 degrees, the frequency deviations is increased, even the secondary correction performed completely.

[PURPOSE OF THE INVENTION]

The purpose of the invention is to perform stable, wide-range temperature compensation without the above-described disadvantages.

[ABSTRACT]

FIG. 2 shows a block diagram according to the present invention. The analog output of a temperature detecting circuit 207 is converted into digital information by an A-D converting circuit 206. An error of the temperature detecting circuit and an error of the A-D converting circuit are added to the information, so it is corrected into digital data as to each integrated circuit chip. This corrected value is written in a storage circuit 202 composed of an EPROM (Erasable Programmable Read Only Memory) and so on temporarily, and the corrected data is stored in a primary and secondary correction circuit 203. After the data is converted on axial symmetry basis about the peak temperature of crystal, thereby, making primary and secondary corrections. The primary correction substitutes the tertiary correction. The high order 3-4 bits of the obtained binary data are led to a frequency dividing circuit 205 as they are to perform speeding-up and slowing -down operation. The low order bits is converted to the duty cycle of the output pulse as they are to perform switching a constant of capacity and a feedback resistor of an crystal oscillation circuit 204. By temperature compensation system, the highly accuracy under the wide-range of temperature can be kept when it is assumed that observed frequency would be an average value of the certain time (for example, 10 seconds).

[EMBODIMENT]

FIG.3 shows an embodiment according to the present invention. A block 301, corresponded to a block 201 in FIG.2, is a temperature information correction circuit. The followings are respectively corresponded to FIG.2, that is, 302 (corresponded to 202) is a storage circuit, 303 (corresponded to 203) is a primary and secondary correction circuit of a quartz-crystal oscillator, 304 (corresponded to 204) is an oscillation circuit, 305 (corresponded to 205) is a frequency dividing circuit. With the output form the A-D converter, the cycle is in proportion to the temperature as shown in FIG. 4. When the output is inputted to presettable downcounters 306 and 307, signals having the pulse-width proportional to the numerical code defined in EPROM= 312 can be obtained. Here, by changing the numerical code, the inclination with respect to the temperature can be varied. At an AND gate 308, signals with 16 kHz and signals having pulse-width of (temperature) $\times$ (the numerical code) are added and the temperature information is converted into pulse number with 16 kHz. The signal is further led to the presettable downcounters consisted by 309-311 so as to perform the counting of the pulse number.

Here, the down-count is operated, the pulse number is adjusted to be 0 at the peak temperature of crystal (the peak temperature due to secondary characteristic of crystal) in EPROM 312. Further, as shown in FIG. 5, it is also adjusted to be the same temperature information at the point distant from the peak temperature by the same temperature.

Next, when it is assumed that this information is n, in the quartz-crystal oscillator primary, secondary correction circuit 303, n is converted into n (n + k) in the temperature higher than the peak temperature and n is

converted into n (n - k) in the temperature lower than the peak temperature as described below.

315 and 316 are program frequency dividing circuits. When the temperature information is n, they are operated as n frequency dividing circuits. In 319, both addition and subtraction of k are performed according to the output from a counter 311. Accordingly, 317 and 318 are operated as the frequency dividing circuits of (n + k) (n - k), in a comprehensive way, it is carried out an calculation of n (n + k), n (n ÷ k). Since the square processing is performed in this calculation, original data is assumed to be m bit, it becomes 2m bits length. Thus, an AND gate 320 is provided for discarding the lower-order m bits and for taking out the higher-order m bits. The final data becomes as shown in Fig 6 and is converted into binary code to be stored in upcounters 321-324. the middle and lower-order bits obtained data controls feedback resistors 325 and 326 of the crystal oscillation circuit 304 as they are to change the gain and perform the adjustment of the output frequency. Also, the high-order 3-4 bits of the obtained binary data are led to the frequency dividing circuit 305 as they are to perform logical speeding-up and slowing-down operation.

Frequency - temperature characteristics by the present temperature compensation system is given by as following formula.

$$f = \beta (T - \theta_{MAX})^2 + r (T - \theta_{MAX})^3 - A$$

$$A = N1 \times 3.05 \times 10^{-6} + N_2/2m \times 3.05 \times 10^{-6}$$

Here,

β: secondary temperature coefficient of quartz-crystal oscillator

r: tertiary temperature coefficient of quartz-crystal oscillator

N_1: high-order bit value of final corrected value

N_2: low-order bit value of final corrected value

θ MAX: peak temperature

[EFFECT]

As the effect of the present system, the following can be described. Firstly, by positively using a storage circuit, the increasing of area can be prevented compared with using the FUSE method. FAMOS (Floating-gate Avalanche injection Metal Oxide Semiconductor) is used as EPROM, and frequency dividing circuits provided inside are used for accessing these address. For this reason, when data is written into FAMOS, one high voltage applying terminals is enough by making last terminal to serve as the terminal.

Secondary, the primary correction substitutes a simply correction of tertiary temperature coefficient of the quartz-crystal oscillator. In a temperature in the range of θ MAX with plus or minus 10 degrees, the tertiary temperature coefficient does not cause a problem, however, when the temperature in the excess of θ MAX with plus or minus 20 degrees, the frequency deviations due to the tertiary coefficient is drastically increased. According to the present system, high accuracy can be maintained even over a wide range of temperature.

Thirdly, frequency is corrected in the crystal oscillation circuit and the frequency dividing circuit. When the frequency is corrected only in the crystal oscillation circuit, the large capacity switching is required, so that electric power consumption of the oscillation circuit is increased and switching noise is mixed, which causes the circuit to be unstable. Also, when the frequency is corrected by speeding-up and slowing-down operation only in the frequency dividing circuit, correction timing is equal to or more than 2-3 minutes, therefore, when it is applied as a timepiece body, the normal quartz tester can not be used. According to the present system, correction is

performed in the both circuits, so that stable oscillation circuit, high accuracy over a wide temperature range, and easy maintenance can be realized.

4. BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a block diagram of conventional highly accurate electronic timepiece circuit;

FIG.2 is a block diagram according to the present invention;

FIG.3 is a circuit diagram showing an embodiment according to the present invention;

FIG.4 is a diagram showing a characteristic of temperature sensor;

FIG.5 is a diagram showing an output characteristic of a temperature information correction circuit; and

FIG.6 is a diagram showing an output characteristic of first and secondary correction circuit of a quartz-crystal oscillator.

101, 204, 304.... crystal oscillation circuit

102, 205, 305... frequency dividing circuit

103, 207...temperature detecting circuit

104, 206...A-D converter circuit

105, 201, 301...temperature information correction circuit

106...pulse-width-modulation circuit

202, 302...storage circuit

203, 303...first and secondary correction circuit of quartz-crystal oscillator

306, 307, 309-311, 313,

314-318, 321-324, 330, 331.... flip-flop

308, 320...AND circuit

312...FAMOS

325, 326...MOS transistor

327...inverter

328...quartz-crystal oscillator

329...resistance

Patent Applicant Kabushiki Kaisha Suwa Seikosha

Agent Patent attorney Tsutomu Mogami

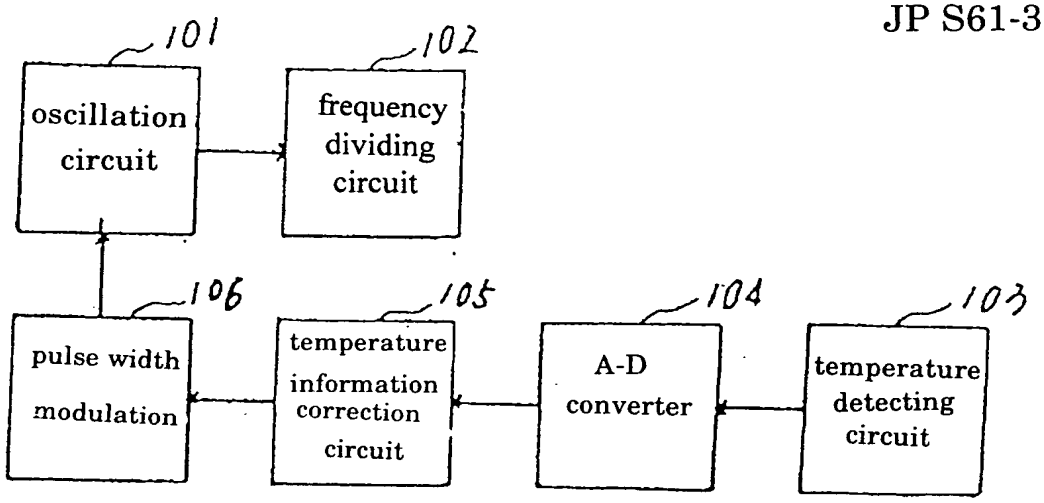
101
oscillation circuit
102
frequency dividing circuit
106
pulse width modulation
105
temperature information correction circuit
104
A-D converter
103
temperature detecting circuit

FIG. 1

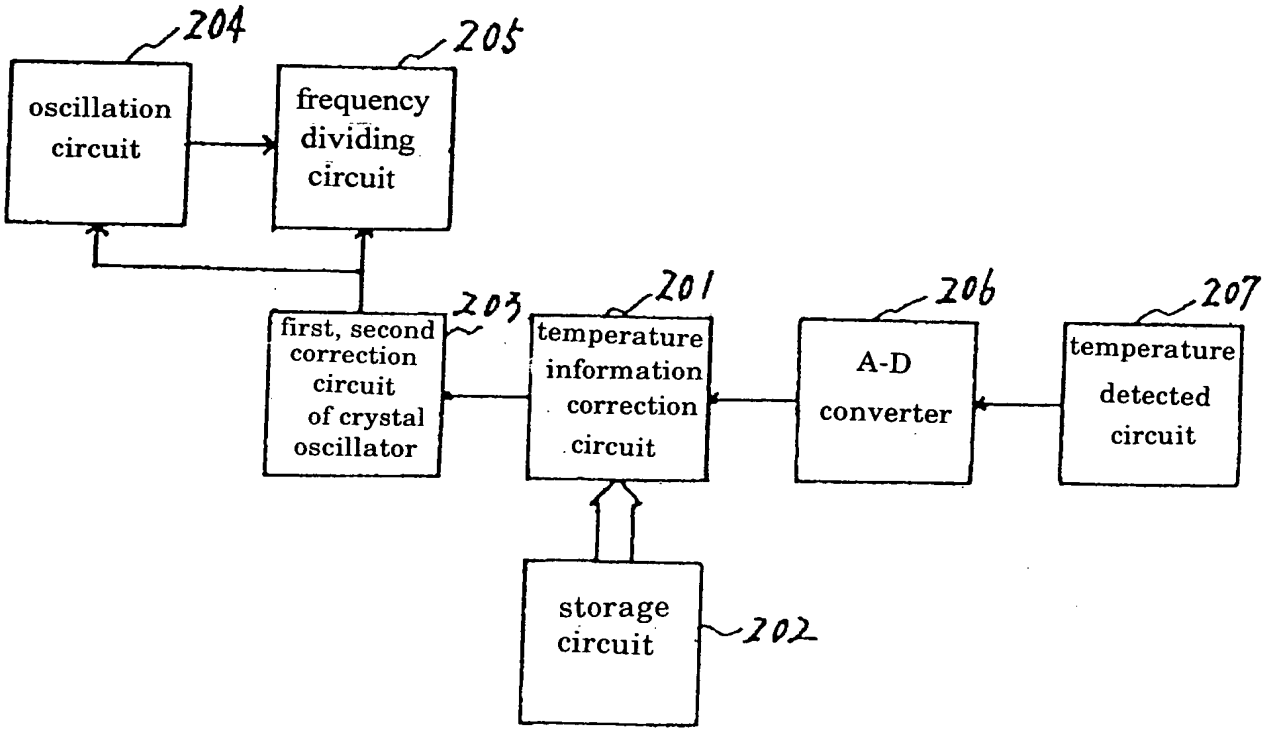
204
oscillation circuit
205
frequency dividing circuit
203
first, second correction circuit of crystal oscillator
201
temperature information correction circuit
206
A-D converter
207
temperature detected circuit
storage circuit
202

FIG. 2

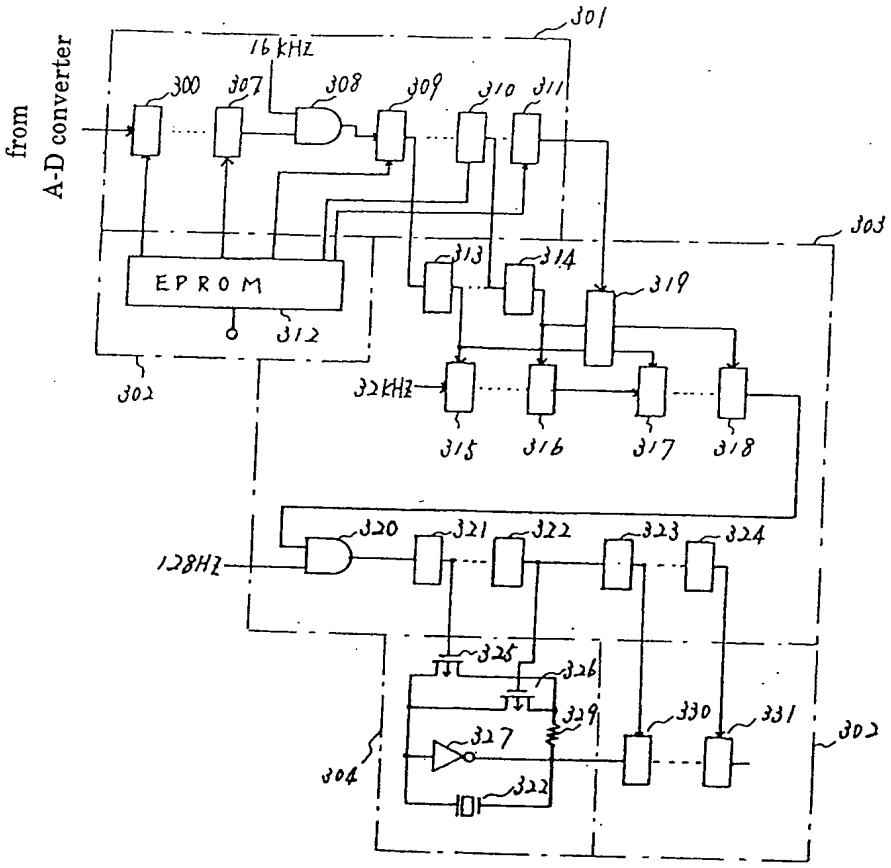

FIG. 3

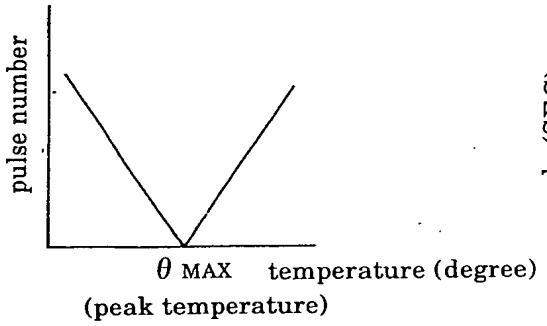

FIG. 5

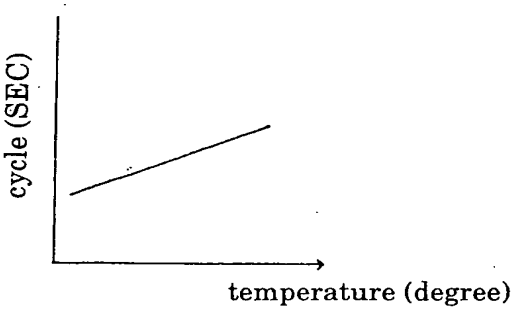

FIG. 4

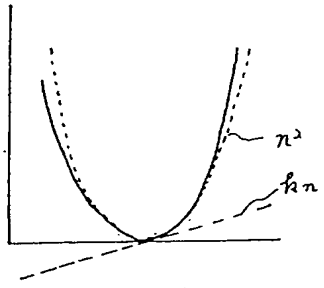

FIG. 6

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⑤1Int.Cl.⁴　識別記号　庁内整理番号　⑬公開　昭和61年(1986)2月15日
H 03 B 5/32　A－6749－5J

審査請求　未請求　発明の数 1　（全4頁）

⑤4発明の名称　温度補償形電子時計

⑳特　願　昭59－154794
㉒出　願　昭59(1984)7月24日

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明　細　書

1. 発明の名称

温度補償形電子時計

2. 特許請求の範囲

温度検知回路、アナログ温度情報をデジタルに変換するA－Dコンバータ、デジタル情報のバラツキを補正するための温度情報補正で構成される高精度電子時計において、前記温度情報補正回路に対し補正値を与える記憶回路と前記温度情報補正回路の出力データを温度に対する一次，二次などの係数を発生させる論理回路と、前記論理回路の出力のデータに従って周波数が変化する発振回路と、前記論理回路の別なデータに従って論理緩急を行なう分周回路とで構成されたことを特徴とする温度補償形電子時計。

3. 発明の詳細な説明

〔技術分野〕

本発明は水晶振動子の温度による周波数偏差を補正して高精度の電子時計を実現するものである。

〔従来技術〕

第1図に従来の温度補償形高精度時計回路のブロック図を示す。温度検知回路103で温度に比例したアナログ情報をA－D変換回路104でデジタル情報に変換する。その後温度検知回路は個々にバラツキを持つため、温度情報補正回路でバラツキを補正する。時計用32KHzの水晶振動子は温度に対して二次の係数が支配的であるため、パルス巾変調回路106で二乗回路を構成して水晶発振回路の発振周波数を変化させていた。

ところが温度情報は発振回路に帰還されて大きな容量切換を行なうため、発振回路が不安定になり、広い温度範囲での補償が困難であった。また水晶には温度に対する三次特性が含まれ、完全に二次補正を行なったとしても、常温±20℃以上では周波数偏差が大きくなる。

〔目　的〕

本発明はこれらの欠点を除去してより安定で広

範囲の温度補償を行なうものである。

〔概　要〕

第２図は本発明によるブロック図である。温度検知回路２０７からのアナログ出力はＡ－Ｄ変換回路２０６でデジタル情報に変換される。この情報は温度検知回路の誤差、Ａ－Ｄ変換回路の誤差が加算されるため、集積回路１チップずつデジタルデータに補正を行なう。この補正値は一旦ＥＰＲＯＭ（Erasable Programmable Read Only Memory）などで構成される記憶回路２０２に書き込まれ補正されたデータは一次，二次補正回路２０３で記憶される。水晶の頂点温度に対して線対称に変換された後、一次，二次補正を行なう。一次補正は三次補正の代用とする。ここで得られたバイナリのデータの上位３～４ビットは、そのまま分周回路２０５に導き論理緩急を行なう。下位数ビットはパルスのdutyに変換して、発振回路２０４の容量、帰還抵抗などの定数の切換を行なう。これらの温度補償システムは周波数をある時間（例えば１０秒）の平均値として観測したとき、広い温度範囲にわたって高い精度を保つ。

〔実施例〕

第３図に本発明の実施例を示す。ブロック３０１は第２図でのブロック２０１に対応し温度情報補正回路である。以下それぞれ第２図に対応し３０２（＝２０２）は記憶回路、３０３（＝２０３）は水晶振動子一次，二次補正回路、３０４（＝２０４）は発振回路、３０５（＝２０５）は分周回路である。Ａ－Ｄ変換器からの出力は第４図に示したように周期が温度に比例している。この出力をプリセッタブル・ダウンカウンタ３０６，３０７に入力すると、ＥＰＲＯＭ＝３１２で設定した数値コードに比例したパルス巾を持つ信号が得られる。ここでは数値コードを変化させることにより温度に対する傾きを可変することができる。ＡＮＤゲート３０８で１６ＫＨｚの信号と（温度）×（数値コード）のパルス巾の信号は加算され、温度情報は１６ＫＨｚのパルス数に変換される。この信号は更に３０９～３１１で構成されるプリセッタブル・ダウンカウンタに導かれてパルス数のカウントを行なう。

ここでダウンカウントを行なう際、頂点温度（水晶のもつ二次特性の頂点の温度）のときパルス数が０となるような調整をＥＰＲＯＭ３１２で行なう。更に第５図に示すように頂点温度に対して同じ温度だけ離れると同一温度情報となるような調整も行なう。

次にこの情報をｎとすると水晶振動子一次二次補正回路３０３において、以下に述べるように頂点温度より高い温度ではｎ（ｎ＋ｋ）、頂点温度より低い温度ではｎ（ｎ－ｋ）に変換される。３１５，３１６はプログラム分周回路である。温度情報がｎの場合はｎ分周回路として働く。３１９はカウンタ３１１の出力に従ってｋの加算および、減算を行なう。従って３１７，３１８は（ｎ＋ｋ）（ｎ－ｋ）の分周回路として動作し、総合的にみるとｎ（ｎ＋ｋ），ｎ（ｎ＋ｋ）の演算を行なったことになる。この演算では二乗処理をするため、元のデータをｍビットとすると２ｍビットの長さになってしまう。このため下位ｍビットを切り捨て、上位ｍビットを取り出すようにＡＮＤゲート３２０を設ける。最終データは第６図のようになりバイナリコードでアップカウンタ３２１～３２４に蓄積される。これらのデータ中下位数ビットは水晶発振回路３０４の帰還抵抗３２５，３２６を制御してゲインを変え、出力周波数の調整を行なう。また上位３～４ビットは分周回路３０５に導き論理緩急を行なう。

本温度補償システムによる周波数－温度特性は次の式で与えられる。

$$f=\beta(T-\theta_{MAX})^2+\gamma(T-\theta_{MAX})^3-A$$

$$A=N_1\times3.05\times10^{-6}+\frac{N_2}{2^m}\times3.05\times10^{-6}$$

ここで、

β：水晶振動子二次温度係数

γ：　〃　　三

N_1：最終補正値の上位ビット値

N_2：　〃　　の下位ｍビット値

θ_{MAX}：頂点温度

〔効　果〕

本システムの効果としては次のようなことが掲げられる。一つは記憶回路を積極的に使用したことにより、ＰＵＳＥ法を使用することに対して面積の増加がないことである。ＥＰＲＯＭとしてＦＡＭＯＳ（Floating-Gate Avalanche injection Metal Oxide Semiconductor）を使い、これらのアドレスをアクセスするものとして内部の分周回路を利用した。このためＦＡＭＯＳにデータを書き込む場合、アドレス設定はラスト端子を兼用すると、高電圧印加端子１個でよい。

二つめは水晶振動子の三次温度係数を一次によって簡易補正を行なうことである。θ_{MAX} ±10℃ぐらいの温度範囲では特に三次係数は問題とならないが、θ_{MAX} ±20℃を越えると急激に三次係数による周波数偏差が大きくなる。本システムは広範囲の温度でも高精度を保つ。

三つめは周波数の補正を水晶発振回路と分周回路で行なうことである。水晶発振回路のみで周波数補正を行なうと、大きな容量切換が必要で、発振回路の消費電流の増加、切換ノイズの混入など回路が不安定となる。また分周部だけで論理緩急による周波数補正を行なうと、補正タイミングが２～３分以上となり、時計体とした場合通常のクォーツテスタが使用できない。本システムは両方に補正をかけることにより、より安定な発振回路、広温度範囲にわたる高精度化、さらに簡単なメインテナンスを実現している。

4.　図面の簡単な説明

第１図：従来の高精度電子時計回路のブロック図

第２図：本発明によるブロック図

第３図：本発明による実施例を示す回路図

第４図：温度センサの特性を示す図

第５図：温度情報補正回路出力特性を示す図

第６図：水晶振動子の一次，二次補正回路の出力特性を示す図

１０１，２０４，３０４…水晶発振回路

１０２，２０５，３０５…分周回路

１０３，２０７…温度検知回路

１０４，２０６…Ａ－Ｄ変換回路

１０５，２０１，３０１…温度情報補正回路

１０６…パルス巾変調回路

２０２，３０２…記憶回路

２０３，３０３…水晶振動子一次二次補正回路

３０６，３０７，３０９～３１１，３１３，３１４～３１８，３２１～３２４，３３０，３３１……フリップフロップ

３０８，３２０…ＡＮＤ回路

３１２…ＦＡＭＯＳ

３２５，３２６…ＭＯＳトランジスタ

３２７…インバータ

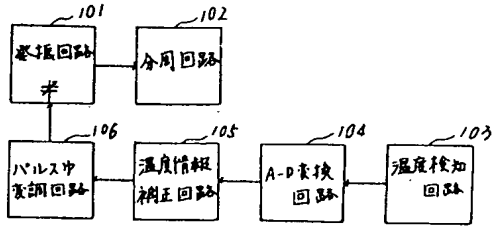
３２８…水晶振動子

３２９…抵抗

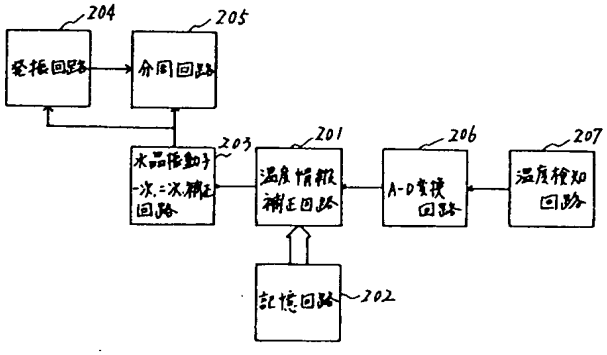
以　上

出願人　　株式会社諏訪精工舎

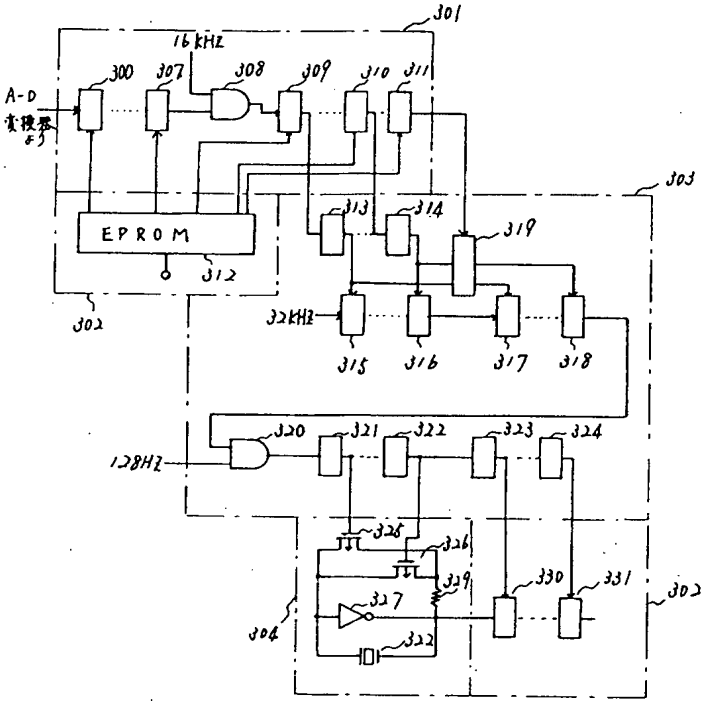
代理人　　弁理士　最　上　　務



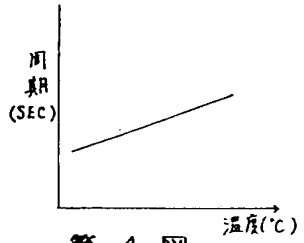
第１図



第２図



第 3 図



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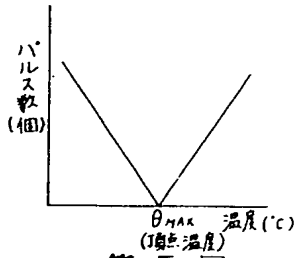
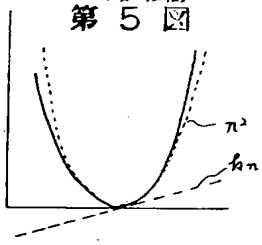


第 5 図



第 6 図